REMARKS

Claims 1-7, 9-13 and 15-19 remain pending in this application.

Claims 1, 9-11, 13 and 15-19 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassell et al. (U.S. Patent No. 6,208,650; hereinafter Hassell) in view of Springer et al. (U.S. Patent No. 4,247,920; hereinafter Springer). The rejection is respectfully traversed.

Claim 1 recites a network device that includes a plurality of receive devices and an external memory interface. Claim 1 recites that the external memory interface includes a first external memory bus to transfer data to a first memory and a second external memory bus to transfer data to a second memory, where the external memory interface is further configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the second external memory bus.

The Final Office Action essentially repeats the previous rejection and admits that Hassell does not disclose an external memory interface as recited in claim 1 (Final Office Action – pages 2-3). The Final Office Action, however, states that Springer discloses an external memory interface that includes an even memory and an odd memory and points to col. 1, lines 63-67 for support (Final Office Action – page 3). The Final Office Action further states that Springer discloses that the external memory interface includes a first external memory bus and a second external memory bus and that the external memory interface is configured to generate odd address information when transferring data via the first external memory bus and even address information when transferring data via the

2

second external memory bus and points to col. 5, line 34 to col. 6, line 6 for support (Final

Office Action – page 3). The applicants respectfully disagree.

Initially, the applicants note that it is not clear what element(s) in Springer are

alleged to be equivalent to the claimed external memory interface. The applicants

respectfully request that any subsequent communication particularly point out what

element(s) in Springer are alleged to be equivalent to the claimed external memory interface

so that the applicants can fully understand the alleged correlation between Springer and the

claim features.

In any event, as discussed in the previous response, Springer is directed to a system

for permitting individual bytes of a two-byte information signal to be stored or retrieved

from a single memory space (Springer – col. 1, lines 40-58). Springer at col. 1, lines 63-67

discloses that a memory device may be divided into two modules, one designated odd and

the other designated even to indicate a logical grouping of addresses. Springer at col. 5, line

6 to col. 6, line 6 discloses performing a 16-bit memory access to memory modules 22 and

24 (Fig. 1). Springer discloses that a 16-bit memory access will result in an access to both

modules 22 and 24 at a module address of N/2 if N is even and access to module 22 at an

address defined by an integer part of N/2 and an access to module 24 at an address defined

by the integer part of (N+1)/2 if N is odd (col. 5, lines 27-33 and Fig. 1). Therefore,

Springer discloses that access to modules 22 and 24 is based on receipt of an address signal

N on address signal line 34 (See col. 2, lines 60-68 and Fig. 1).

Springer is clearly not directed to transferring data from receive devices that

correspond to ports on a network device. Springer, therefore, cannot disclose an external

memory interface that transfers data received from a first receive device (that corresponds to

a port) to a first memory and transfers data received from a second receive device (that

corresponds to a port) to a second memory, as required by claim 1.

Springer further does not disclose an external memory interface that is configured to

generate odd address information when transferring data via the first external memory bus

and even address information when transferring data via the second external memory bus.

Springer, in contrast, merely discloses that the system of Fig. 1 provides access to even or

odd memory based on an address on signal line 34.

In response to these arguments, the Final Office Action states that Springer discloses

"the ability to write 8 bit data addressed to an odd memory space into an odd memory, to

write 8 bit data addressed to even memory into an even memory, and to write a 16 bit word

into 8 bit additions to the even and odd memories" and points to col. 5, lines 37-53 and Figs.

1 and 2 for support (Final Office Action – pages 8-9). The Final Office Action further states

that "when the scheduler stores odd addressed data, that data gets sent across the memory

bus that corresponds to odd memory, and the same with even addressed memory, this is the

same as generating odd address information via the first memory bus as seen in the

specification on page 7, line 24 to page 8, line 7" (Final Office Action – page 9). The

applicants respectfully disagree.

Writing odd addressed words into an odd address memory and even addressed words

into an even memory, as disclosed by Springer, is simply not equivalent to and does not

suggest the use of an external memory interface that is configured to receive data from a

plurality of receive devices (where the receive devices are configured to receive data frames

from stations and the receive devices correspond to ports on a network device) and generate

odd address information when transferring data via a first external memory bus and generate

4

even address information when transferring data via a second external memory bus. That is, the mere use of odd addresses and even address, as disclosed in Springer, does not disclose or suggest the use of an external memory interface, as recited in claim 1.

For at least the reasons discussed above, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 1.

In addition, even if, for the sake of argument, the combination of Hassell and Springer could be fairly construed to disclose or suggest each of the features of claim 1, the Final Office Action does not provide the requisite motivation under 35 U.S.C. § 103 as to why it would have been obvious to combine Hassell and Springer.

For example, the Final Office Action states that it would have been obvious to use Springer's teaching in Hassell's switch "in order to have memory modules that are accessible in parallel (Column 1, lines 63-65) without having a more complex addressing system (Column 2, lines 28-33)" (Final Office Action – page 3). The applicants respectfully disagree.

Hassell is directed to a circuit for performing high-speed low latency frame relay switching (Hassell – Abstract). Springer, in contrast, is directed to a method for permitting the transfer of a two-byte information signal into and out of a storage area (Springer – Abstract). These two references are unrelated other than the fact that both include memory devices. The Examiner's motivation statement for combining these disparate references is merely a conclusory statement providing an alleged benefit of the combination. Such motivation does not satisfy the requirements of 35 U.S.C. § 103.

Further, the portions of Springer to which the Final Office Action points, apparently as providing motivation for the combination, (col. 1, lines 63-65 and col. 2, lines 28-33)

merely disclose that a memory device is divided into two parallel accessible modules and

that transferring a two-byte signal may be accomplished without regard to whether the first

bytes being addressed is odd or even. These portions of Springer also do not provide

objective motivation as to why it would have been obvious to combine Springer with

Hassell.

For at least these reasons, withdrawal of the rejection and allowance of claim 1 are

respectfully requested.

Claim 9 is dependent on claim 1 and is believed to be allowable for at least the

reasons claim 1 is allowable. Accordingly, withdrawal of the rejection and allowance of

claim 9 are respectively requested.

Claim 10 recites a method for storing data frame information that includes

simultaneously transferring data frame information to at least a first memory and a second

memory, wherein the simultaneously transferring includes alternately transferring data

frame information from a first group of the receive devices to the first and second memories

and alternately transferring data frame information from a second group of the receive

devices to the first and second memories.

The Final Office Action effectively admits that Hassell does not disclose these

features, but states that Springer discloses these features and points to col. 2, lines 1-11 for

support (Final Office Action – page 4). The applicants respectfully disagree.

As discussed in the previous response, Springer at col. 2, lines 1-11 discloses:

For an even memory address N, an access is made to a location in each memory
module having an address of N/2. For an odd memory address N, the access in the odd
module is to a location having an address defined by the integer part of N/2, but the
access in the odd module is to a location having an address defined by the integer part

of N/2+1. In the first case, the even memory module supplies or receives the upper byte of the information signal, and in the second case, the odd module supplies or receives the upper byte.

This portion of Springer merely discloses how to process an incoming address signal N with respect to an odd and even memory module. This portion of Springer clearly does not disclose alternately transferring data frame information from a first group of the receive devices to the first and second memories and alternately transferring data frame information from a second group of the receive devices to the first and second memories, as recited in claim 10.

In response to this argument, the Final Office Action states that the applicants are attempting to argue the art individually and not the combination (Final Office Action – page 9). The applicants strongly disagree with the characterization of the previous arguments and maintain that the Examiner has not addressed the features recited in claim 10.

First, claim 10 recites that the simultaneously transferring includes <u>alternately transferring data frame information from a first group of the receive devices to the first and second memories</u> and <u>alternately transferring data frame information from a second group of the receive devices to the first and second memories</u>.

Springer may disclose the use of an odd and even memory, which are apparently considered by the Examiner to be equivalent to the claimed first and second memories. However, the mere fact that Hassell discloses use of odd and even addressed memories cannot be fairly construed to disclose or suggest the claimed features. That is, the Final Office Action has not pointed out where Springer allegedly discloses alternately transferring data frame information from a first group of devices to the odd and even memories in Springer, as required by claim 10 (based on the alleged equivalence of the odd and even

memories to the claimed first and second memories). The Final Office Action has also not pointed out where Springer discloses or suggests alternately transferring data frame information from a second group of receive devices to the odd and even memories in Springer, as further required by claim 10 (based on the alleged equivalence of the odd and even memories to the claimed first and second memories).

Therefore, the applicants have not argued the references individually, but merely pointed out the deficiencies in the combination of Hassell and Springer with respect to the features recited in claim 10.

The last sentence on page 9 of the Final Office Action is also unclear ("when Hassell devices to store a data frame from the first memory onto the external memory it can be sent to both external memories simultaneously, and the same for the second receive device, thus giving the functionality of alternatively sending data from both receiving devices to both memories at once"). This statement provides no additional support for the notion that either Hassell or Springer discloses or suggests the features discussed above.

For at least these reasons, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 10.

In addition, the applicants further assert that the motivation to combine Hassell and Springer does not satisfy the requirements of 35 U.S.C. § 103 for the reasons discussed above with respect to claim 1.

For at least these reasons, withdrawal of the rejection and allowance of claim 10 are respectfully requested.

Claims 11, 13 and 15 are dependent on claim 10 and are believed to be allowable for at least the reasons claim 10 is allowable. In addition, these claims recite additional features not disclosed or suggested by the cited art.

For example, claim 11 recites simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices. The Final Office Action states that Springer discloses this feature and points to col. 2, lines 18-27 for support (Final Office Action – page 4). The applicants respectfully disagree.

As discussed in the previous response, Springer at col. 2, lines 18-27 discloses that an objective of Springer's invention is to provide means for transferring a two-byte information signal into and out of a byte-oriented memory system such that the first and second bytes are associated with sequential storage locations. This portion of Springer clearly does not disclose simultaneously transmitting selection signals to first and second receive devices for selectively outputting data stored in the first and second receive devices, as recited in claim 11.

The applicants note that this argument was made in the previous response and was not addressed in the Final Office Action. The applicants respectfully request that this argument be addressed in any subsequent communication or the rejection be withdrawn. The applicants also note that a similar feature is recited in claim 2. The Final Office Action with respect to claim 2 admits that neither Hassell nor Springer discloses simultaneously outputting first and second selection signals for outputting data from the first and second receive devices (Final Office Action – page 6). The applicants, therefore, respectfully

request clarification as to the grounds of rejection. In any event, the combination of Hassell and Springer does not disclose or suggest the feature recited in claim 11.

For at least this additional reason, withdrawal of the rejection and allowance of claim 11 are respectfully requested.

Claim 16 recites a data communication system that includes a plurality of receive devices, a scheduler, a switching device, a first memory and a second memory. Claim 16 recites that the scheduler is configured to generate selection signals to selectively output data frame information from the receive devices. The Final Office Actions states that Hassell discloses this feature and points to col. 6, lines 37-52 for support (Final Office Action – page 5). The applicants respectfully disagree.

Hassell at col. 6, lines 37-52 discloses:

The circuit has a memory management block 130 comprised of a look up table (LUT) 131 having a parameter table 132, a buffer allocation functional block 133, a buffer allocation table 134, and a free buffer pointer 136. The circuit 40 also has a frame buffer descriptor (FBD) table 140 and a queue memory 150. The queue memory 150 has an input queue 151 (shown in FIGS. 4 and 6) associated with the input queue pointer 114, an output queue 152 (shown in FIGS. 4-6) associated with the output queue pointer 121, as well as a free queue list 153 having an associated free queue pointer 154 (shown in FIG. 6).

The input and output queues of the queue memory 150, and the frame buffers associated with the buffer allocation table 134 are constructed as linked lists. A linked list is a data structure in which each item of the list consists of a data component and a pointer or link to the next item in the list.

This portion of Hassell does not disclose or suggest a scheduler that is configured to generate selection signals to selectively output data frame information from the receive devices, as recited in claim 16. In contrast, this portion of Hassell merely discloses the use of a queue memory having an input queue and an output queue.

Claim 16 also recites a switching device configured to receive the data frame information and to simultaneously transfer data frame information from a first one of the

data frames via a first external memory bus and data frame information from a second one

of the data frames via a second external memory bus. The Final Office Action states that

Springer discloses these features and points to col. 2, lines 1-11 for support (Final Office

Action – page 5). The applicants respectfully disagree.

As discussed above, Springer at col. 2, lines 1-11 discloses

For an even memory address N, an access is made to a location in each memory
module having an address of N/2. For an odd memory address N, the access in the odd
module is to a location having an address defined by the integer part of N/2, but the
access in the odd module is to a location having an address defined by the integer part
of N/2+1. In the first case, the even memory module supplies or receives the upper
byte of the information signal, and in the second case, the odd module supplies or
receives the upper byte.

This portion of Springer, however, does not disclose a switching device that receives

data frame information (output from the receive devices), transfers data frame information

from a first data frame and transfers data frame information from a second data frame, much

less that the transferring is done simultaneously. In contrast, this portion of Springer merely

discloses processing associated with receiving a signal having an address N on signal line

34.

Claim 16 also recites that the switching device is further configured to generate data

address information having odd addresses for data transferred to the first memory and

generate data address information having even addresses for data transferred to the second

memory. The Final Office Action states that Springer discloses these features and points to

col. 5, line 34 to col. 6, line 6 for support (Final Office Action – page 5). The applicants

respectfully disagree.

Similar to the discussion above with respect to claim 1, this portion of Springer does

not disclose generating odd addresses for data transferred to a first memory and even

11

addresses for data transferred to a second memory, as recited in claim 16. Rather, Springer merely discloses using existing address information received on address signal line 34 to determine a module address associated with accessing memory modules 22 and 24.

For at least these reasons, the combination of Hassell and Springer does not disclose or suggest each of the features of claim 16.

In addition, the applicants further assert that the motivation to combine Hassell and Springer does not satisfy the requirements of 35 U.S.C. § 103 for the reasons discussed above with respect to claim 1.

For at least these reasons, withdrawal of the rejection and allowance of claim 16 are respectfully requested.

Claims 17-19 are dependent on claim 16 and are believed to be allowable for at least the reasons claim 16 is allowable. In addition, these claims recite additional features not disclosed or suggested by the cited art.

For example, claim 18 recites that the switching device is further configured to alternately transfer data received from the first multiplexer to the first and second external memory buses and to alternately transfer data received from the second multiplexer to the first and second external memory buses. The Final Office Action states that Springer discloses this feature and points to col. 2, lines 1-11 for support (Final Office Action – page 6). The applicants respectfully disagree.

Springer at col. 2, lines 1-11, as discussed above, merely discloses how to process incoming address signals N with respect to an odd and even memory module. This portion of Springer, however, does not even disclose the use of first and second multiplexers, much less alternately transferring data received from the first multiplexer to the first and second

external memory buses and alternately transferring data received from the second

multiplexer to the first and second external memory buses, as required by claim 18.

For at least these additional reasons, withdrawal of the rejection and allowance of

claim 18 are respectfully requested.

Claims 2-6 and 12 have been rejected under 35 U.S.C. § 103(a) as being

unpatentable over Hassell in view of Springer and further in view of Gayton et al. (U.S.

Patent No. 5,680,401; hereinafter Gayton). The rejection is respectfully traversed.

Claims 2-6 and 12 depend on claims 1 and 10, respectively, and are believed to be

allowable for at least the reasons their respective independent claims are allowable. Gayton

does not make up for the deficiencies in the combination of Hassell and Springer discussed

above with respect to claims 1 and 10. In addition, these claims recite additional features

not disclosed or suggested by the cited art.

For example, claim 2 recites that the external memory interface includes a scheduler

coupled to the receive devices and configured to enable the received data frames to be

output to the first and second memories, the scheduler simultaneously outputting first and

second selection signals for outputting data from the first receive device and the second

receive device, respectively.

The Final Office Action admits that neither Hassell nor Springer discloses these

features. The Final Office Action, however, states that Gayton discloses a scheduler that

allows two memories to operate and deal with two different receive devices separately and

simultaneously and points to col. 5, lines 16-18 for support (Final Office Action – page 6).

Gayton at col. 5, lines 16-18 discloses that TX buffer memory 46 provides 32 bits of

data to TX FIFO 28 and RX buffer memory 45 reads 32 bits of data from RX FIFO 30 at

every cycle of the clock signal. This portion of Gayton, however, does not disclose a scheduler that <u>simultaneously outputs first and second selection signals for outputting data from the first receive device and the second receive device, respectively,</u> as recited in claim 2.

For at least these additional reasons, withdrawal of the rejection and allowance of claim 2 are respectfully requested.

Claim 4 recites that the external memory interface is further configured to simultaneously transfer the portions of the data from the first and second receive devices to the first and second memories. The Final Office Action states that Gayton discloses this feature and points to col. 5, lines 16-18 for support (Final Office Action – page 7). The applicants respectfully disagree.

Gayton at col. 5, lines 16-18, as discussed above, merely discloses that TX buffer memory 46 provides 32 bits of data to TX FIFO 28 and RX buffer memory 45 reads 32 bits of data from RX FIFO 30 at every cycle. This portion of Gayton clearly does not disclose or suggest simultaneously transferring the portions of the data from the first and second receive devices to the first and second memories, as recited in claim 4.

For at least these additional reasons, withdrawal of the rejection and allowance of claim 4 are respectfully requested.

Claim 6 recites that the external memory interface is further configured to alternately transfer data received from the first group of receive devices to the first and second memories and to alternately transfer data received from the second group of receive devices to the first and second memories. The Final Office Action states that Springer discloses this

feature and points to col. 2, lines 1-11 for support (Final Office Action – pages 7-8). The applicants respectfully disagree.

Similar to the discussion above with respect to claim 10, Springer at col. 2, lines 1-11 does not disclose or suggest alternately transferring data received from a first group of devices to the first and second memories or alternately transferring data received from a second group of devices to the first and second memories, as recited in claim 6.

For at least these additional reasons, withdrawal of the rejection and allowance of claim 6 are respectfully requested.

Claim 7 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hassell in view of Springer in view of Gayton and further in view of Runaldue et al. (U.S. Patent No. 6,052,751; hereinafter Runaldue). The rejection is respectfully traversed.

Claim 7 depends on claim 5 and is believed to be allowable for at least the reasons claim 1 is allowable. Runaldue does not make up for the deficiencies in the combination of Hassell, Springer and Gayton discussed above with respect to claim 1. Accordingly, withdrawal of the rejection and allowance of claim 7 are respectfully requested.
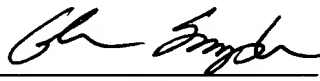

CONCLUSION

In view of the foregoing remarks, the applicants respectfully request withdrawal of the outstanding rejections and the timely allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, please feel free to call the undersigned attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136

is hereby made. Please charge any shortage in fees due in connection with the filing of this

paper, including extension of time fees, to Deposit Account 50-1070 and please credit any

excess fees to such deposit account.

Respectfully submitted,

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